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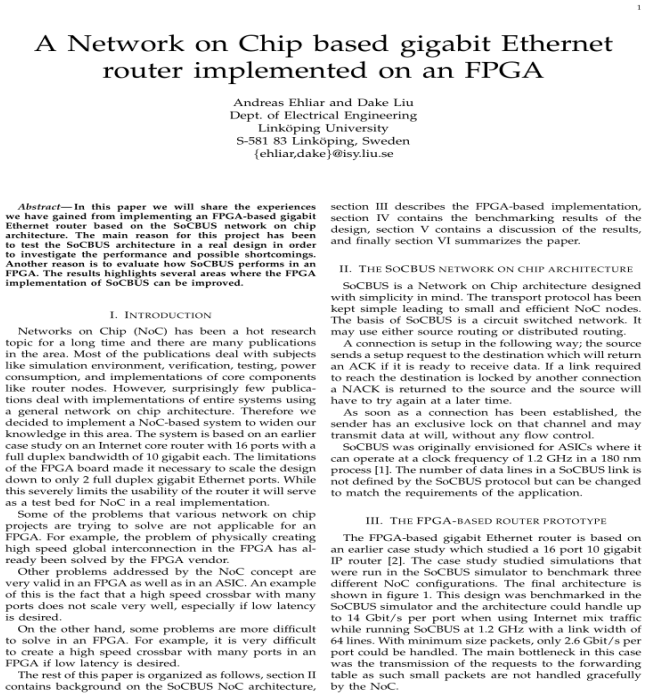

A Network on Chip based gigabit Ethernet router implemented on an FPGA

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***Abstract*— In this paper we will share the experiences we have gained from implementing an FPGA-based gigabit Ethernet router based on the SoCBUS network on chip architecture. The main reason for this project has been to test the SoCBUS architecture in a real design in order to investigate the performance and possible shortcomings. Another reason is to evaluate how SoCBUS performs in an FPGA. The results highlights several areas where the FPGA implementation of SoCBUS can be improved.**

I. Introduction

Networks on Chip (NoC) has been a hot research topic for a long time and there are many publications in the area. Most of the publications deal with subjects like simulation environment, verification, testing, power consumption, and implementations of core components like router nodes. However, surprisingly few publications deal with implementations of entire systems using a general network on chip architecture. Therefore we decided to implement a NoC-based system to widen our knowledge in this area. The system is based on an earlier case study on an Internet core router with 16 ports with a full duplex bandwidth of 10 gigabit each. The limitations of the FPGA board made it necessary to scale the design down to only 2 full duplex gigabit Ethernet ports. While this severely limits the usability of the router it will serve as a test bed for NoC in a real implementation.

Some of the problems that various network on chip projects are trying to solve are not applicable for an FPGA. For example, the problem of physically creating high speed global interconnection in the FPGA has already been solved by the FPGA vendor.

Other problems addressed by the NoC concept are very valid in an FPGA as well as in an ASIC. An example of this is the fact that a high speed crossbar with many ports does not scale very well, especially if low latency is desired.

On the other hand, some problems are more difficult to solve in an FPGA. For example, it is very difficult to create a high speed crossbar with many ports in an FPGA if low latency is desired.

The rest of this paper is organized as follows, section II contains background on the SoCBUS NoC architecture, section III describes the FPGA-based implementation, section IV contains the benchmarking results of the design, section V contains a discussion of the results, and finally section VI summarizes the paper.

II. The SoCBUS network on chip architecture

SoCBUS is a Network on Chip architecture designed with simplicity in mind. The transport protocol has been kept simple leading to small and efficient NoC nodes. The basis of SoCBUS is a circuit switched network. It may use either source routing or distributed routing.

A connection is setup in the following way; the source sends a setup request to the destination which will return an ACK if it is ready to receive data. If a link required to reach the destination is locked by another connection a NACK is returned to the source and the source will have to try again at a later time.

As soon as a connection has been established, the sender has an exclusive lock on that channel and may transmit data at will, without any flow control.

SoCBUS was originally envisioned for ASICs where it can operate at a clock frequency of 1.2 GHz in a 180 nm process [1]. The number of data lines in a SoCBUS link is not defined by the SoCBUS protocol but can be changed to match the requirements of the application.

III. The FPGA-based router prototype

The FPGA-based gigabit Ethernet router is based on an earlier case study which studied a 16 port 10 gigabit IP router [2]. The case study studied simulations that were run in the SoCBUS simulator to benchmark three different NoC configurations. The final architecture is shown in figure 1. This design was benchmarked in the SoCBUS simulator and the architecture could handle up to 14 Gbit/s per port when using Internet mix traffic while running SoCBUS at 1.2 GHz with a link width of 64 lines. With minimum size packets, only 2.6 Gbit/s per port could be handled. The main bottleneck in this case was the transmission of the requests to the forwarding table as such small packets are not handled gracefully by the NoC.

Results 1 - 25 of Fifth International Workshop on System-on-Chip for Real-Time Applications (IWSOC'05). July Ottawa, Ont., Canada (4). Dept. of Electr. & Comput. Eng., Alberta Univ., Edmonton, Alta., Canada (4) Banff, Alberta, Canada (7). Banff, Alta., Canada (2) Applications, Proceedings.Published in: Fifth International Workshop on System-on-Chip for Real-Time Applications (IWSOC'05). Article #. Date of Conference: July IEEE International Workshop on System-on-Chip for Real-Time Applications ; 5; ; for Real-Time Applications: 20 - 24 July , Banff, Alberta, Canada.The 5th IEEE International Workshop on System-on-Chip for Real-Time Applications. July Banff, Alberta - Canada. Edited by. Wael Badawy, Dept. of.Proceedings of the 5th IEEE International Workshop on for Real-Time Applications (IWSOC), July , Banff, Alberta, Canada.IEEE International Workshop on System-on-Chip for Real-Time Applications Applications: proceedings: July, , Calgary Alberta, Canada by IEEE for Real-Time Applications: proceedings: July, , Banff, Alberta, Canada by Audience level: (from for IWSOC to for Fifth Inte).A system on chip (SoC) can provide an integrated solution to challenging design .. in on-chip networks, Proceedings of the 23rd International Conference on Real Time and . on Chips, IEEE Design & Test, v n.5, p, September .. on Circuits, Signals and Systems, July , , Banff, Alberta, Canada.Effects of Oil on Wildlife: Proceedings of the Eighth International Conference. St. John's, Newfoundland, Canada: August 3?5, . EUB Alberta Energy and Utilities Board Statistical Series Alberta Coal Industry Monthly Statistics Data up to .. An Integrated System for Real Time Calculation and Visualization of.Computer Engineering (CCECE), pages , Toronto, Canada, May .. In Proceedings of the 5th IEEE International Workshop on System-on-Chip for Real-Time Applications (IWSOC), July , Banff, Alberta., Second prize - best poster, IEEE International Radar Conference, on System-on-Chip for Real Time Applications, Banff, Alberta, Canada, July , , Best Paper Award, The 5th World Multiconference on Systemics, . on System on a Chip (IWSOC), Banff, Alberta Canada, July , Conference: Conference: Proceedings of the 5th IEEE International Workshop on System-on-Chip for Real-Time Applications (IWSOC), July , Banff, Alberta, Canada. Cite this publication. Daniel Eidenskog at Swedish Defence Research Agency. Daniel Eidenskog. ; Swedish Defence.A Cross-Disciplinary Approach for Modeling the Real World, pages , Internet of Things applications, Proceedings of 10th International Conference on . International Symposium on System-on-Chip, Tampere, Finland, October 31 Procedia Computer Science, volume 5, pages , Niagara Falls, Canada.1. INTRODUCTION. The increasing complexity of signal processing systems in .. (IWSOC), July, Banff, Alberta, Canada, pp. [5] Tamer S.CFV ' Fifth International Workshop on Constraints in Formal Verification, Sydney, Australia, August ISOCC ' International SoC Design Conference, Seoul, Korea, October 20 - 21, Proceedings Chair Workshop on System-on-Chip for Real-Time Applications, Banff, Alberta, Canada , July , FIFTH IN TERNATIONAL WORKSHOP ON BANFF, AB, CANADA JULY USA,IEEE LNKD- DOI/IWSOC, 20 July (), pages 92 WORKSHOP

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